IN THE CLAIMS:

Please amend claims 1 and 11 as indicated in the following.

Please add claims 23-26 as indicated in the following.

Please cancel claims 10 and 20 without prejudice as indicated in the following.

Claims Listing:

1. (Currently Amended) A static random access memory (SRAM) device capable of storing a program that is accessible when said SRAM device is powered up, said SRAM device comprising a plurality of storage cells, each of said storage cells comprising:

a data latch having a first input/output (I/O) line and a second I/O line, said data latch comprising:

a first inverter having an input coupled to said first I/O line and an output coupled to said second I/O line; and

a second inverter having an input coupled to said second I/O line and an output coupled to said first I/O line; and

a biasing circuit capable of forcing at least one of said first and second I/O lines to a known logic state when power is applied to said SRAM device, wherein said known logic state comprises a portion of said program, said biasing circuit comprising a grounding circuit selectively connected by a programmable connect to one of said first inverter output and said second inverter output, wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device, thereby grounding one of said first inverter output and said second inverter output and forcing said second I/O line to said known logic state.

2. (Original) The SRAM device as set forth in Claim 1 wherein said biasing circuit initially applies power only to said first inverter.

3. (Original) The SRAM device as set forth in Claim 2 wherein said initial application of power only to said first inverter forces said first inverter output to a Logic 1 state.

4. (Original) The SRAM device as set forth in Claim 3 wherein said biasing circuit subsequently applies power to said second inverter.

5. (Original) The SRAM device as set forth in Claim 4 wherein said subsequent application of power to said second inverter forces said second inverter output to a Logic 0 state.

6. (Original) The SRAM device as set forth in Claim 1 wherein said biasing circuit initially applies power only to said second inverter.

7. (Original) The SRAM device as set forth in Claim 6 wherein said initial application of power only to said second inverter forces said second inverter output to a Logic 1 state.

8. (Original) The SRAM device as set forth in Claim 7 wherein said biasing circuit subsequently applies power to said first inverter.

9. (Original) The SRAM device as set forth in Claim 8 wherein said subsequent application of power to said first inverter forces said first inverter output to a Logic 1 state.

10. (Canceled)

11. (Currently Amended) A data processor comprising a central processing unit (CPU) capable of executing a boot-up program when power is applied to said CPU, said CPU comprising:

a static random access memory (SRAM) device capable of storing said boot-up program, said SRAM device comprising a plurality of storage cells capable of storing said boot-up program, each of said storage cells comprising:

a data latch having an input and an output, said data latch comprising:

a first inverter having an input coupled to said first I/O line and an output coupled to said second I/O line; and

a second inverter having an input coupled to said second I/O line and an output coupled to said first I/O line; and

a biasing circuit capable of forcing at least one of said first and second I/O lines to a known logic state when power is applied to said SRAM device, wherein said known logic state comprises a portion of said boot-up program, said biasing circuit comprises a grounding circuit selectively connected by a programmable connect to one of said first inverter output and said second inverter output, wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device, thereby grounding one of said first inverter output and said second inverter output and forcing said second I/O line to said known logic state.

12. (Original) The data processor as set forth in Claim 11 wherein said biasing circuit initially applies power only to said first inverter.

13. (Original) The data processor as set forth in Claim 12 wherein said initial application of power only to said first inverter forces said first inverter output to a Logic 1 state.

14. (Original) The data processor as set forth in Claim 13 wherein said biasing circuit subsequently applies power to said second inverter.

15. (Original) The data processor as set forth in Claim 14 wherein said subsequent application of power to said second inverter forces said second inverter output to a Logic 0 state.

16. (Original) The data processor as set forth in Claim 11 wherein said biasing circuit initially applies power only to said second inverter.

17. (Original) The data processor as set forth in Claim 16 wherein said initial application of power only to said second inverter forces said second inverter output to a Logic 1 state.

18. (Original) The data processor as set forth in Claim 17 wherein said biasing circuit subsequently applies power to said first inverter.

19. (Original) The data processor as set forth in Claim 18 wherein said subsequent application of power to said first inverter forces said first inverter output to a Logic 1 state.

20. (Canceled)

21. (Canceled)

22. (Canceled)

23. (New) The SRAM device as set forth in Claim 1 wherein said grounding circuit comprises a first transistor comprising a first node coupled to a voltage reference, a second node selectively connected by the programmable connect to one of said first inverter output and said second inverter output and a gate node operable to receive a signal to temporarily enable the grounding circuit after power is applied to said SRAM device.

24. (New) The SRAM device as set forth in Claim 23 wherein said grounding circuit further comprises a second transistor comprising a first node coupled to the voltage reference, a second node selectively connected by a second programmable connect to one of said first inverter output and said second inverter output and a gate node operable to receive the signal to temporarily enable the grounding circuit after power is applied to said SRAM, wherein said second node of said first transistor and said second node of said second transistor are selectively coupled to different outputs of said first inverter output and said second inverter output and wherein said second transistor is an opposite bias type as said first transistor.

25. (New) The data processor as set forth in Claim 11 wherein said grounding circuit comprises a first transistor comprising a first node coupled to a voltage reference, a second node selectively connected by the programmable connect to one of said first inverter output and said second inverter output and a gate node operable to receive a signal to temporarily enable the grounding circuit after power is applied to said SRAM device.

26. (New) The data processor as set forth in Claim 25, wherein said grounding circuit further comprises a second transistor comprising a first node coupled to the voltage reference, a second node selectively connected by a second programmable connect to one of said first inverter output and said second inverter output and a gate node operable to receive the signal to temporarily enable the grounding circuit after power is applied to said SRAM, wherein said second node of said first transistor and said second node of said second transistor are selectively coupled to different outputs of said first inverter output and said second inverter output and wherein said second transistor is an opposite bias type as said first transistor.